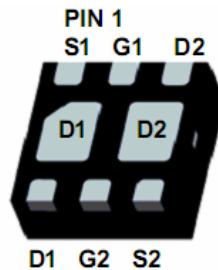


WCM2001

N- and P-Channel Complementary, 20V, MOSFET

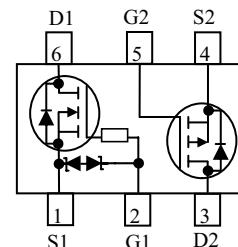
[Http://www.willsemi.com](http://www.willsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ. (mΩ)
N-Channel 20 V	180 @ 4.5V
	225 @ 2.5V
	280 @ 1.8V
P-Channel -20 V	85 @ -4.5V
	110 @ -2.5V
	150 @ -1.8V



Descriptions

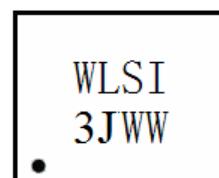
The WCM2001 is the N- and P-Channel enhancement MOS Field Effect Transistor as a single package for DC-DC converter or Load switch applications, uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. Standard Product WCM2001 is Pb-free.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design for extremely low $R_{ds(on)}$
- Exceptional ON resistance and maximum DC current capability
- Small package design with DFN2x2-6L.



WLSI = Company
 3J = Device Code
 WW = Week Code

Marking

Order Information

Device	Package	Shipping
WCM2001-6/TR	DFN2x2-6L	3000/Tape&Reel

Applications

- Driver: Relays, Solenoids, Lamps, Hammers
- Power supply converters circuit
- Load/Power Switching for potable device

Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Unit
V_{DSS}	Drain-to-Source Voltage	20	-20	V
V_{GSS}	Gate-to-Source Voltage	± 6	± 8	V
I_D	Drain Current – Continue Note1	0.65	-3.1	A
	Drain Current – Pulsed ($t < 300\text{us}$, Duty < 2%) Note1	1.4	-4.1	A
P_D	Power Dissipation – Note1	1.5		W
	Power Dissipation – Note2	0.7		
T_J	Operation junction temperature range	150		°C
T_{SG}	Storage temperature range	-55~150		°C

Thermal Resistance Ratings

($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Single Operation		Dual Operation		Unit
		Typ.	Max.	Typ.	Max.	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient – Note1	65	82	52	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient – Note2	145	175	116	140	°C/W

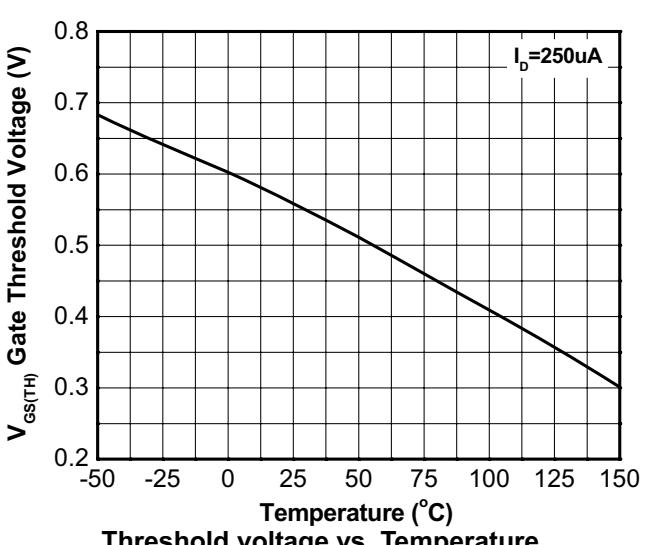
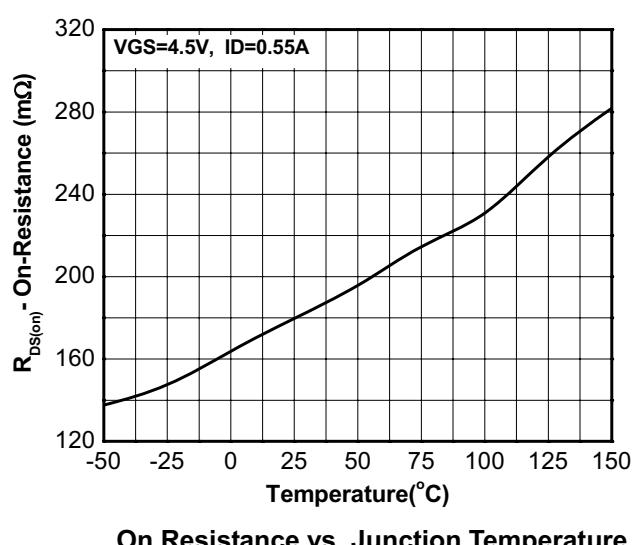
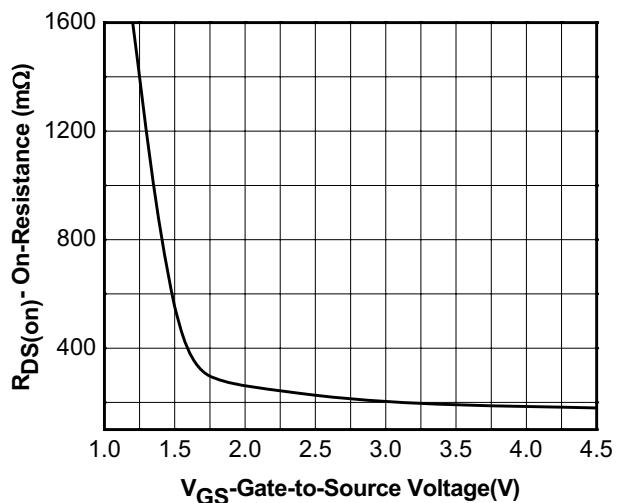
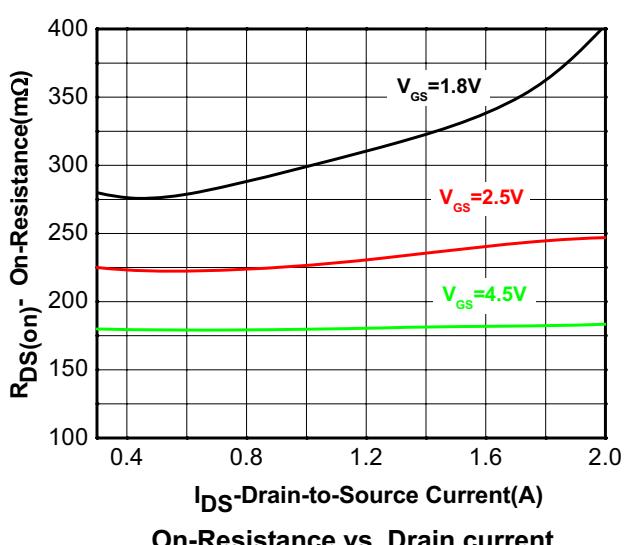
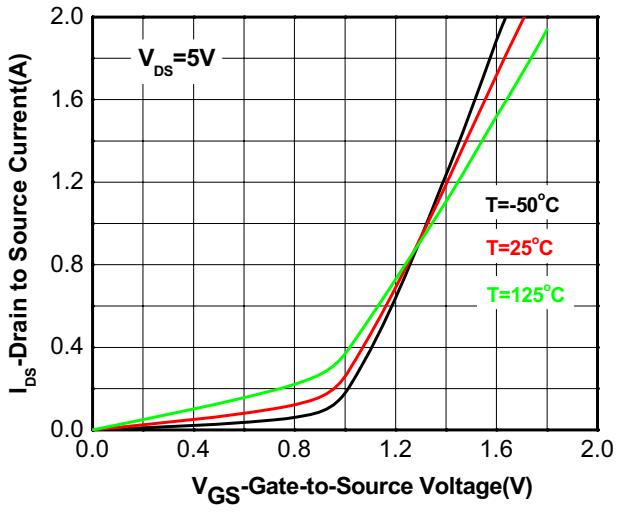
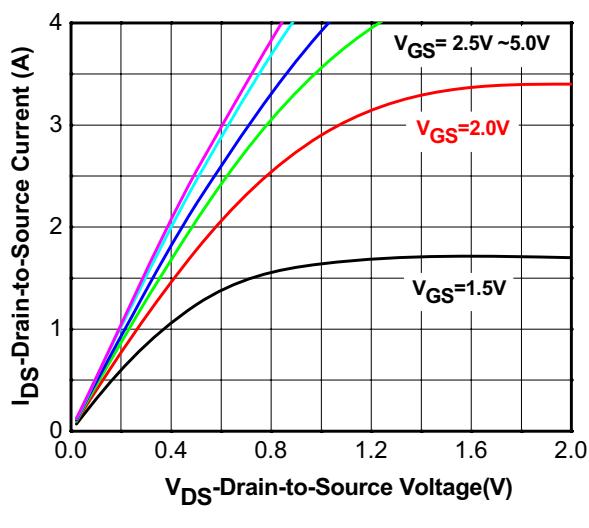
Note1: Surface mounted on a 2 oz copper, 1 in² pad, FR-4 board.

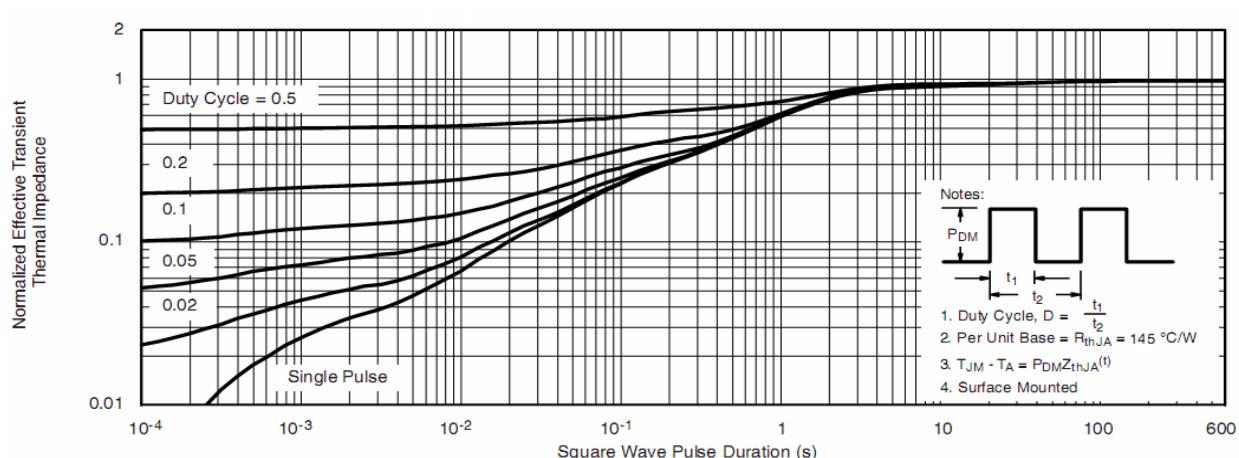
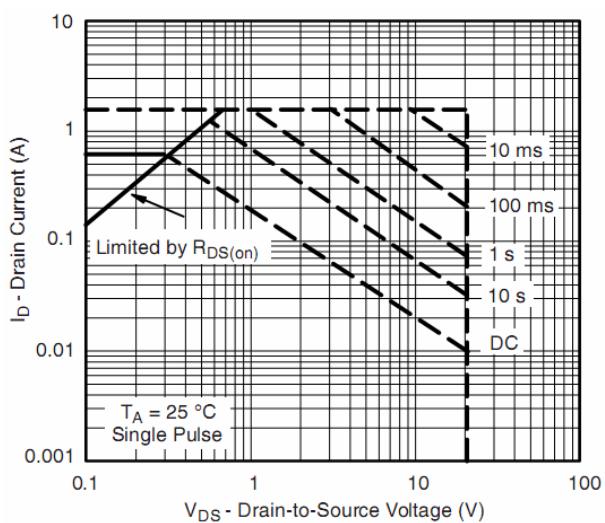
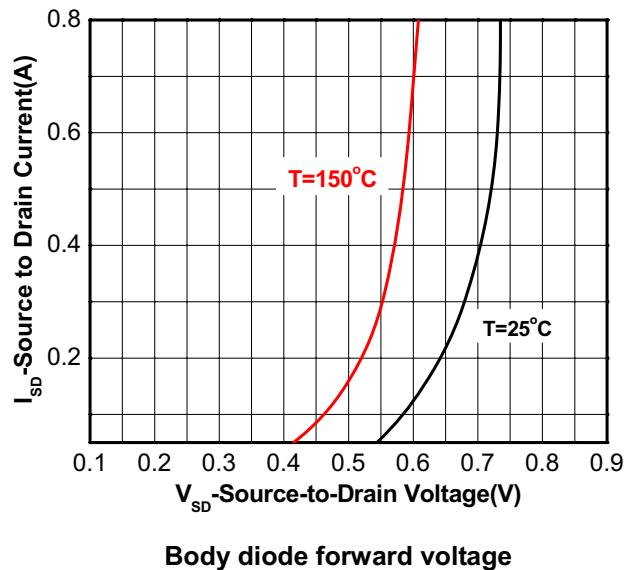
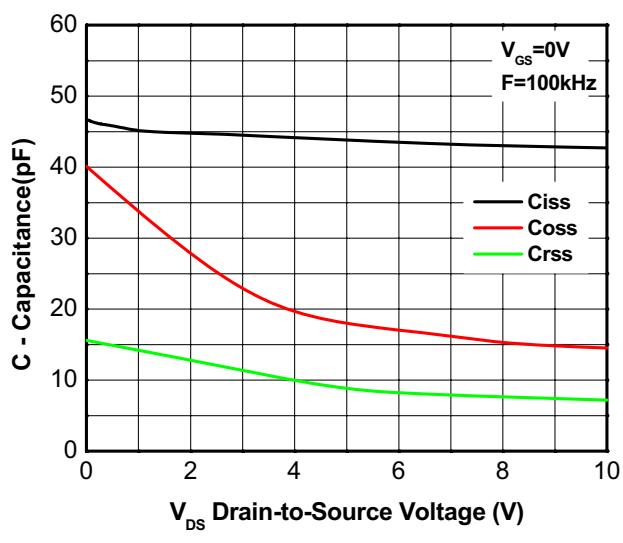
Note2: Surface mounted on a 2 oz copper, minimum pad, FR-4 board

Electronics Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

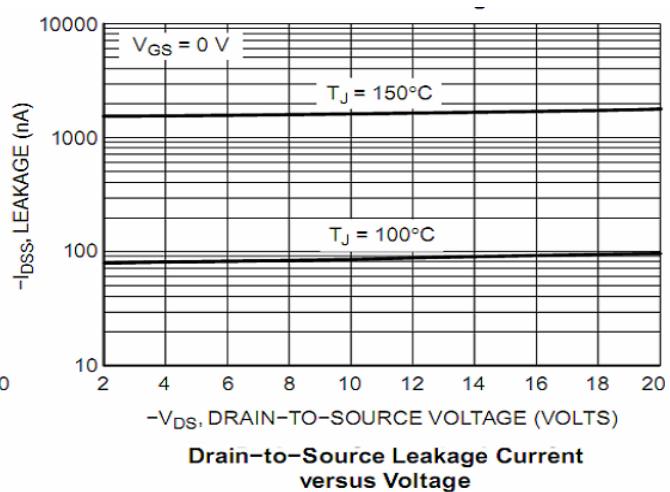
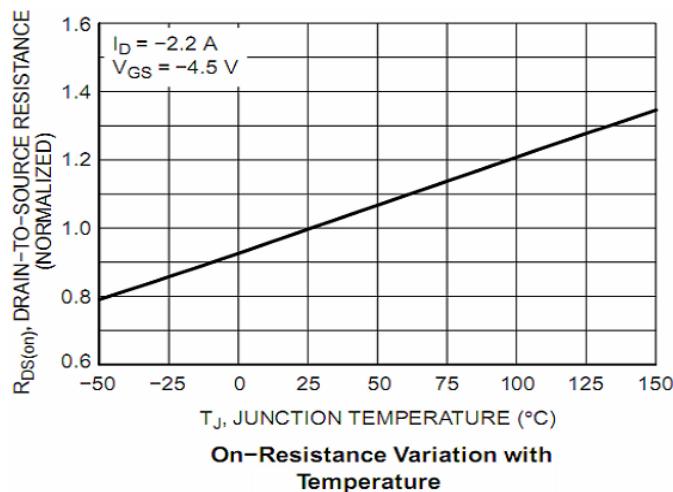
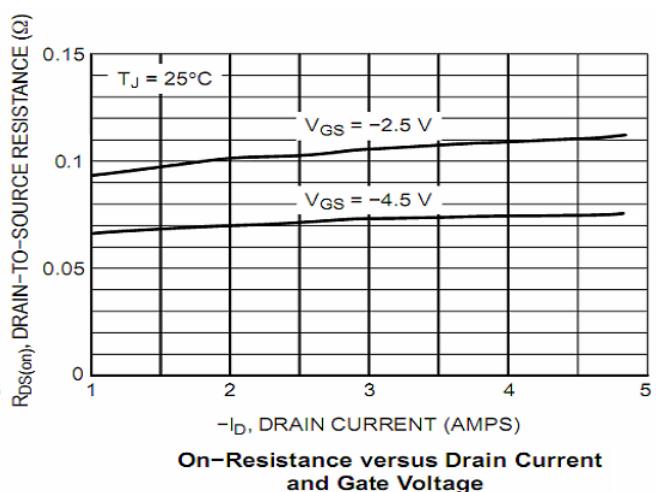
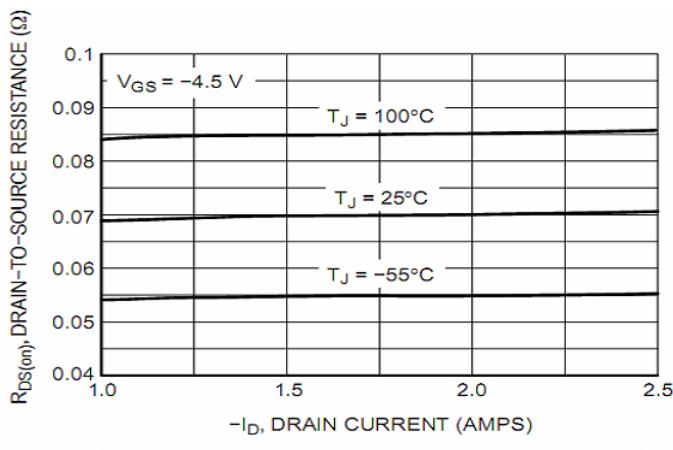
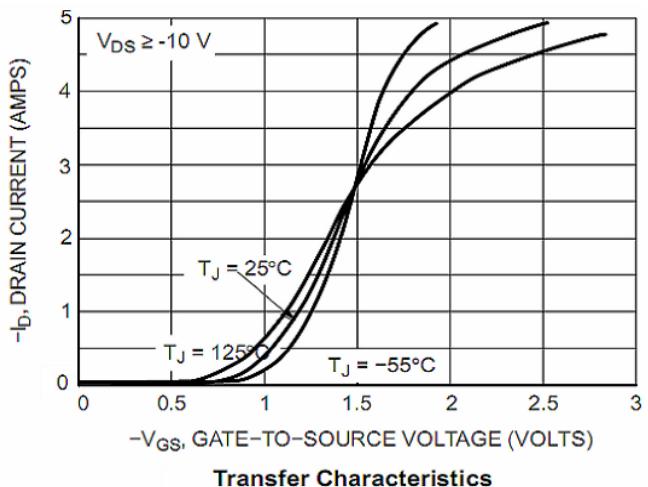
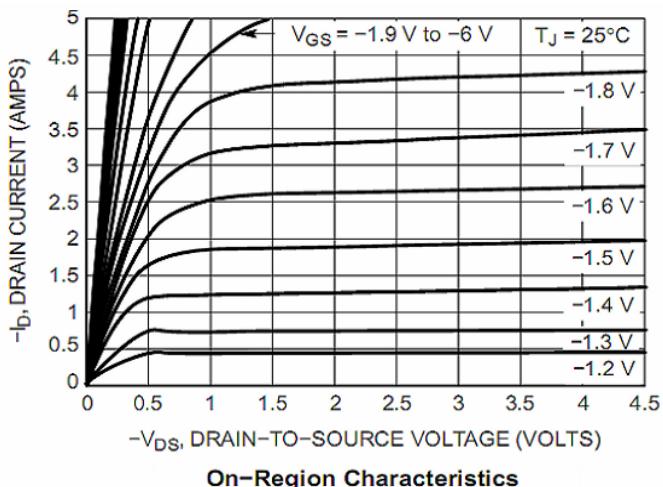
Symbol	Parameter	Test Condition		Min	Typ.	Max	Unit
Off Characteristics							
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$	N-Ch	20			V
		$V_{\text{GS}}=0\text{V}, I_D=-250\mu\text{A}$	P-Ch	-20			
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=16\text{V}, V_{\text{GS}}=0\text{V}$	N-Ch			1	uA
		$V_{\text{DS}}=-16\text{V}, V_{\text{GS}}=0\text{V}$	P-Ch			-1	
I_{GSS}	Gate –Source leakage current	$V_{\text{DS}}=0\text{V}, V_{\text{GS}}=\pm 5\text{V}$	N-Ch			± 5	uA
		$V_{\text{DS}}=0\text{V}, V_{\text{GS}}=\pm 8\text{V}$	P-Ch			± 0.1	
ON Characteristics							
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_D=250\mu\text{A}$	N-Ch	0.4	0.55	0.85	V
		$V_{\text{DS}}=V_{\text{GS}}, I_D=-250\mu\text{A}$	P-Ch	-0.4	-0.56	-1.00	
$R_{\text{DS}(\text{on})}$	Drain-Source On-Resistance	$V_{\text{GS}}=4.5\text{V}, I_D=0.55\text{A}$	N-Ch		180	310	mΩ
		$V_{\text{GS}}=-4.5\text{V}, I_D=-3.1\text{A}$	P-Ch		85	120	
		$V_{\text{GS}}=2.5\text{V}, I_D=0.45\text{A}$	N-Ch		225	360	
		$V_{\text{GS}}=-2.5\text{V}, I_D=-2.8\text{A}$	P-Ch		110	150	
		$V_{\text{GS}}=1.8\text{V}, I_D=0.35\text{A}$	N-Ch		280	460	
		$V_{\text{GS}}=-1.8\text{V}, I_D=-1.5\text{A}$	P-Ch		150	200	
g_{FS}	Forward Transconductance	$V_{\text{DS}} = 5 \text{ V}, I_D = 0.55\text{A}$	N-Ch		2.0		S
		$V_{\text{DS}} = -5 \text{ V}, I_D = -0.45\text{A}$	P-Ch		12		
Dynamic Characteristics							
C_{iss}	Input Capacitance	NMOS: $V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, F=100\text{kHz}$ PMOS: $V_{\text{DS}}=-10\text{V}, V_{\text{GS}}=0\text{V}, F=1\text{MHz}$	N-Ch		50		pF
C_{oss}	Output Capacitance		P-Ch		470		
C_{rss}	Reverse Transfer Capacitance		N-Ch		13		
$Q_{\text{G(TOT)}}$	Total Gate Charge		P-Ch		55		
$Q_{\text{G(TH)}}$	Threshold gate charge		N-Ch		8		
Q_{GS}	Gate-Source Charge		P-Ch		50		
Q_{GD}	Gate-Drain Charge	NMOS: $V_{\text{DS}}=10\text{V}, V_{\text{GS}}=4.5\text{V}, I_D=0.55\text{A}$ PMOS: $V_{\text{DS}}=-10\text{V}, V_{\text{GS}}=-4.5\text{V}, I_D=-2.7\text{A}$	N-Ch		1.15		nC
			P-Ch		6		
			N-Ch		0.06		
			P-Ch		0.34		
			N-Ch		0.15		
			P-Ch		0.75		
			N-Ch		0.23		
			P-Ch		1.2		

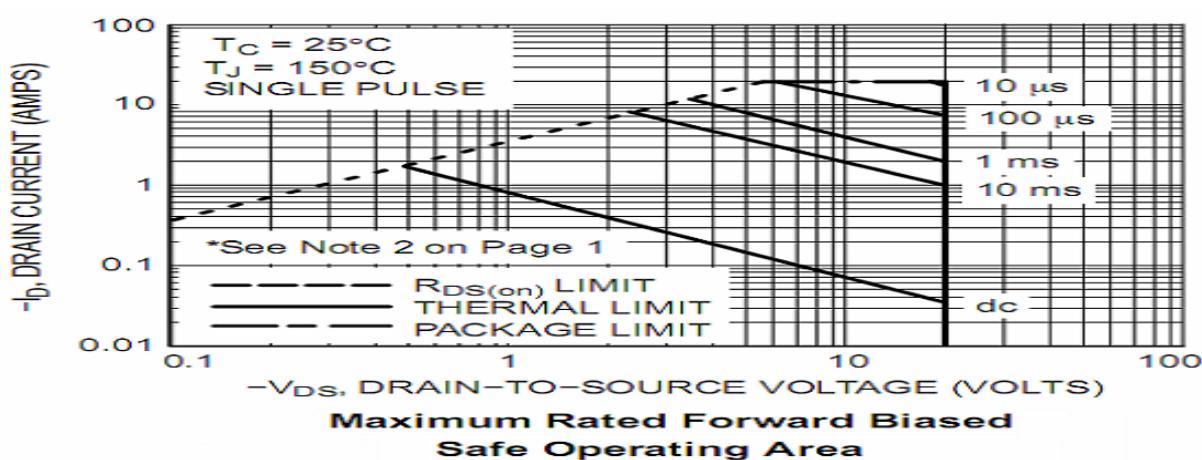
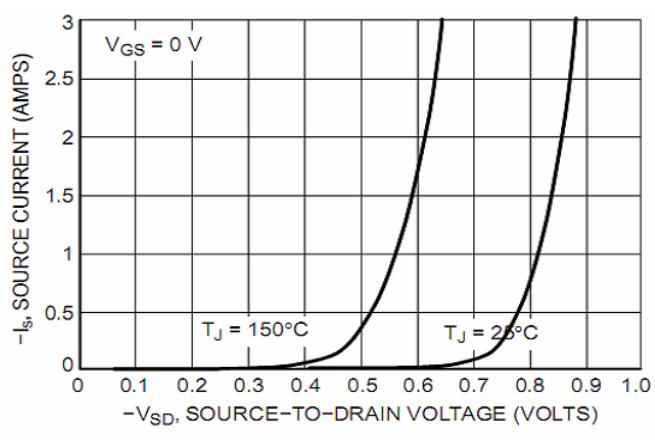
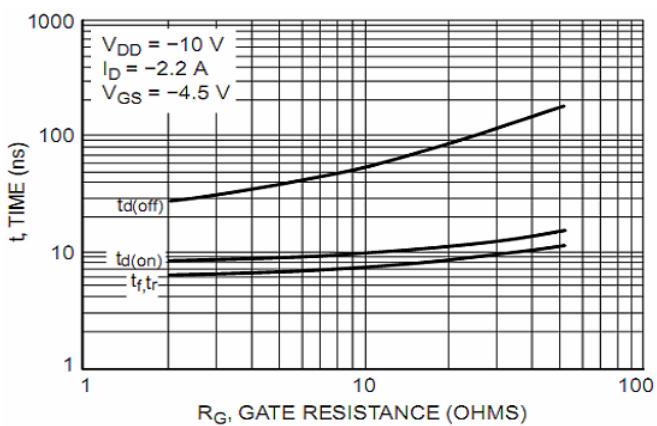
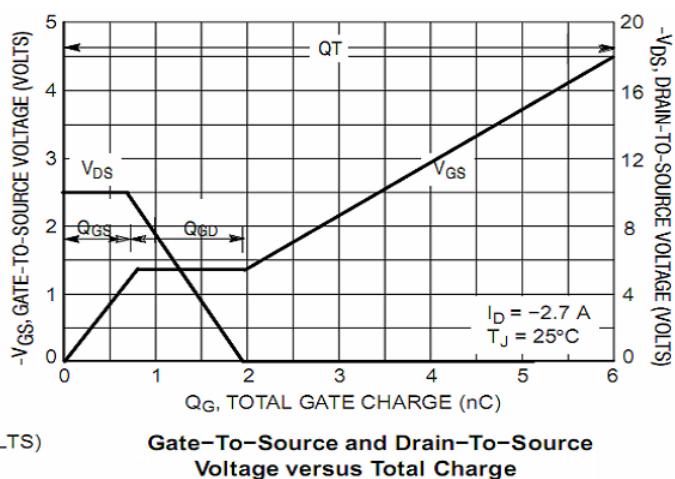
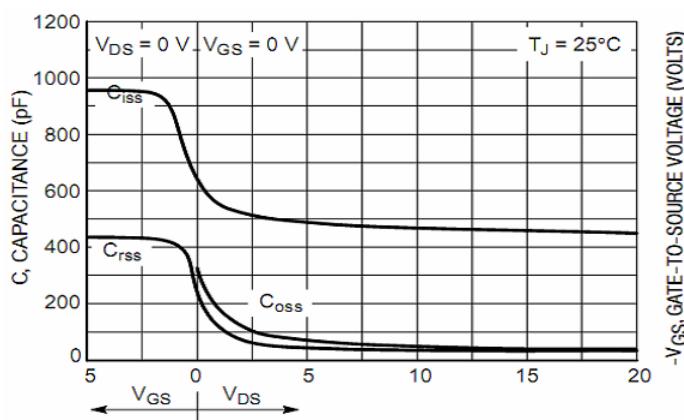
Symbol	Parameter	Test Condition	Min	Typ.	Max	Unit	
Switching Characteristics							
td(on)	Turn-On Delay Time	NMOS: $V_{DD}=10V$, $R_L=18\Omega$, $V_{GEN}=4.5V$, $I_D=0.55A$, $R_G=6\Omega$	N-Ch	22		ns	
tr	Turn-On Rise Time		P-Ch	9			
td(off)	Turn-Off Delay Time		N-Ch	80			
tf	Turn-Off Fall Time		P-Ch	7			
			N-Ch	700			
			P-Ch	40			
			N-Ch	380			
			P-Ch	7			
Drain-to-Source Diode Characteristics							
V_{SD}	Forward Diode Voltage	$V_{GS}=0V$, $I_S=0.15A$	N-Ch	0.5	0.70	1.5	V
		$V_{GS}=0V$, $I_S=-0.9A$	P-Ch	-0.5	-0.70	-1.5	

Typical Performance Graph (N-Channel)




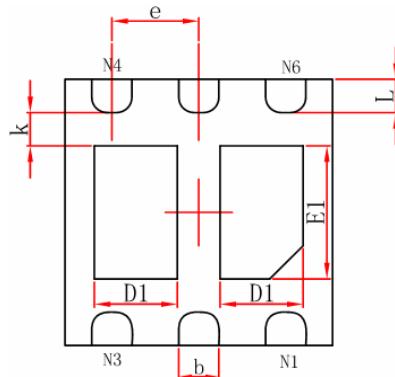
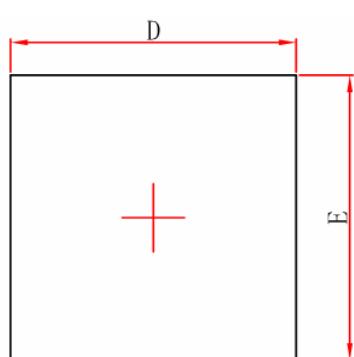
Typical Performance Graph (P-Channel)



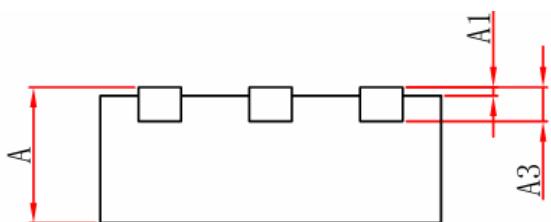


Package Outline Dimension

DFN2x2-6L Dual



Top View



Side View

Symbol	Dimension in Millimeters	
	Min.	Max.
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF	
D	1.924	2.076
E	1.924	2.076
D1	0.520	0.720
E1	0.900	1.100
k	0.200MIN	
b	0.250	0.350
e	0.650TYP	
L	0.174	0.326